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Project Title: A 25 LEVEL ASYMMETRIC MULTILEVEL INVERTER FOR RENEWABLE SOURCES

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TITLE: A 25 LEVEL ASYMMETRIC MULTILEVEL INVERTER FOR RENEWABLE SOURCES

ABSTRACT

In this generation, multilevel inverter is suitable for high-voltage and high-current applications. This project proposes the design and implementation of a 25 level asymmetric inverter using four sources and ten switches. The proposed system consists of four sources which are asymmetrical in nature. Different structures of MLI were developed by researches and academic in order to reduce the switch count and cost. The proposed design is framed by T-type and Cascaded H-bridge MOSFET based voltage source inverter. In this topology staircase output voltage of twenty-five level is generated with minimum components count. This designed topology can be used in various voltage sources by using renewable energy sources to obtain inverted output.

LITERATURE SURVEY

Author details and Title of the paper	Work presented
M. Ye, L. Chen, L. Kang, S. Li, J.Zhang and H. Wu, "Hybrid Multi- Carrier PWM Technique Based on Carrier Reconstruction for Cascaded H-bridge Inverter," in *IEEE Access*, vol. 7, pp. 53152-53162, 2019.	The aforementioned technique uses the carrier segment in the half carrier period of the IPD-PWM technique as the basic unit and optimizes the modulation performance by periodically adjusting its arrangement in the vertical direction. When CHB multilevel inverter adopts Hybrid Multi-carrier PWM technique, as with CPS-PWM technique, the output power balance between the cascaded H-bridge cells is achieved naturally; at the same time, the harmonic spectrum of the output voltage is identical with thatof the IPD-PWM technique, that is to say, the harmonic characteristics of the output line voltage of the inverters are effectively improved.
CM. Ye, W. Ren, L. Chen, Q. Wei, G. Song and S. Li, "Research on Power-Balance Control Strategy of CHB Multilevel Inverter Based on TPWM," in *EEE Access*, vol. 7, pp. 157226-157240, 2019.	By selecting an appropriate trapezoidal wave triangulation rate δ, the modulation strategy can greatly increase the amplitude of the CHB inverter output voltage fundamental wave while ensuring the waveform quality of output phase voltage, and realize the power-balance of H-bridge units within a full modulation ratio range by changing the arrangement of triangular carriers in the vertical direction while using the carrier segment in the half carrier period of the IPD-TPWM strategy as the basicunit.

H. Azeem, S. Yellasiri, V. Jammala, B. S. Naik and A. K. Panda, "A Fuzzy Logic Based Switching Methodology for a Cascaded H-Bridge Multi-Level Inverter," in *IEEE Transactions on Power Electronics*, vol. 34, no. 10, pp. 9360-9364, Oct. 2019.	The proposed technique simplifies the conventional method by eliminating the traditional logic gate design. The fuzzy logic pulse generator acts as alook-up table as well as a pulse generator. Based on the modulation index as input, controlled membership functions (MFs) and rules of the fuzzy logic controller (FLC) opens various possibilities in producing pulses directly. The proposed technique is evaluated on the cascaded multilevel inverter with symmetric and asymmetric operations using selective harmonic elimination pulse width modulation (SHE- PWM).
P. R. Bana, K. P. Panda, R. T. Naayagi, P. Siano and G. Panda, "Recently Developed Reduced Switch Multilevel Inverter for Renewable Energy Integration and Drives Application:Topologies,Comprehensive Analysis and Comparative Evaluation," in *IEEE Access*, vol. 7,pp. 54888-54909, 2019.	To assist with advanced current research in this field and in the selection of suitable inverter for various applications, significant understanding on these topologies is clearly summarized based on the three categories, i.e., symmetrical, asymmetrical, and modified topologies. This review paper also includes a comparison based on important performance parameters, detailed technical challenges, current focus, and future development trends. By a suitable combination of switches, the MLI produces a staircase output with low harmonic distortion.
M. D. Siddique, S. Mekhilef, N. M. Shah and M. A. Memon, "Optimal Design of a New Cascaded Multilevel Inverter Topology with Reduced Switch Count," in *IEEE Access*, vol. 7, pp. 24498-24510, 2019.	Multilevel inverters (MLIs) are a great development for industrial and renewable energy applications due to their dominance over conventional two-level inverter with respect to size, rating of switches, filter requirement, and efficiency. The proposed MLI topology is designed with the aim of reducing the number of switches and the number of dc voltage sources with modularity while having a higher number of levels at the output. For the determination of the magnitude of dc voltage sources and a number of levels in the cascade connection, three different algorithms are proposed.

HARDWARE/SOFTWARE REQUIRED

- Step down transformer
- Battery
- MOSFET(IRF 840)
- Diode
- Resistors
- Microcontroller(PIC 16F877A)

DESIGN AND METHODOLOGY

Using the MatLab simulink the proposed inverter is designed. Fig. 1 gives the topology [16] consist of 8 unidirectional switches from S1 – S8 along with two bidirectional switches from S9 – S10. The proposed topology is asymmetric in nature, magnitude of dc- voltage sources are unequal and are given as V1=V3=Vdc and V2=5Vdc. Using this configuration it can generate 25 output voltage level and the switching state is shown in theTable 1 where – denotes on state and * denotes off state of the switches in the fig 1. Thus 25-L is achieved by below switching sequence. The obtained results from the scope are analyzed.

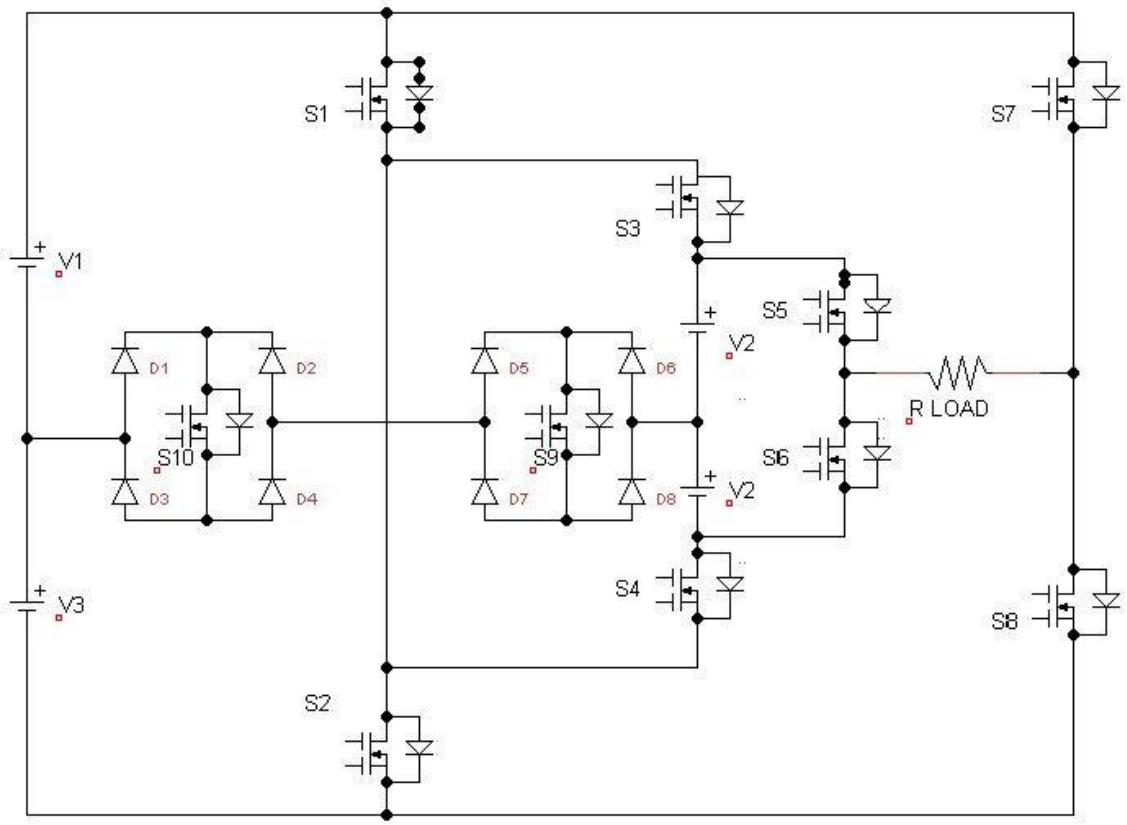


Figure 1.1. Proposed 25 level Topology [16]

Table 2. Switching state for proposed 25 Level topology.

Vo	S1	S2	S3	S4	S5	S6	S7	S8	S9	S10
12Vdc	-	*	*	-	-	*	*	-	*	*
11Vdc	*	*	*	-	-	*	*	-	*	-
10Vdc	-	*	*	-	-	*	-	*	*	*
9Vdc	*	*	*	-	-	*	-	*	*	-
8Vdc	*	-	*	-	-	*	-	*	*	*
7Vdc	-	*	*	*	-	*	*	-	-	*
6Vdc	*	*	*	*	-	*	*	-	-	-
5Vdc	-	*	*	*	-	*	-	*	-	*
4Vdc	*	*	*	*	-	*	-	*	-	-
3Vdc	*	-	*	*	-	*	-	*	-	*
2Vdc	-	*	-	*	-	*	*	-	*	*
Vdc	*	*	-	*	-	*	*	-	*	-

0	-	*	-	*	-	*	-	*	-	-
-Vdc	*	*	*	-	*	-	*	-	*	-
-2Vdc	*	-	*	-	*	-	-	*	*	*
-3Vdc	-	*	*	*	*	-	*	-	-	*
-4Vdc	*	*	*	*	*	-	*	-	-	-
-5Vdc	*	-	*	*	*	-	*	-	-	*
-6Vdc	*	*	*	*	*	-	-	*	-	-
-7Vdc	*	-	*	*	*	-	-	*	-	*
-8Vdc	-	*	-	*	*	-	*	-	*	*
-9Vdc	*	*	-	*	*	-	*	-	*	-
-10Vdc	*	-	-	*	*	-	*	-	*	*
-11Vdc	*	*	-	*	*	-	-	*	*	-
-12Vdc	*	-	-	*	*	-	*	-	*	*

Simulation study and Hardware development

To verify the proposed MLI design, Simulation study has been carried out using MATLAB SIMULINK with R-Load(R=470 ohms). Simulation design output have been shown in Fig 1.2 which as achieved 25 level by connecting four voltage source V1=V3=Vdc and V2=5Vdc and a load resistance of 470 ohms with eight unidirectional switches from S1-S8 and two bidirectional switches from S9-S10 .Thus 25 Level has been achieved by the experimental prototype.

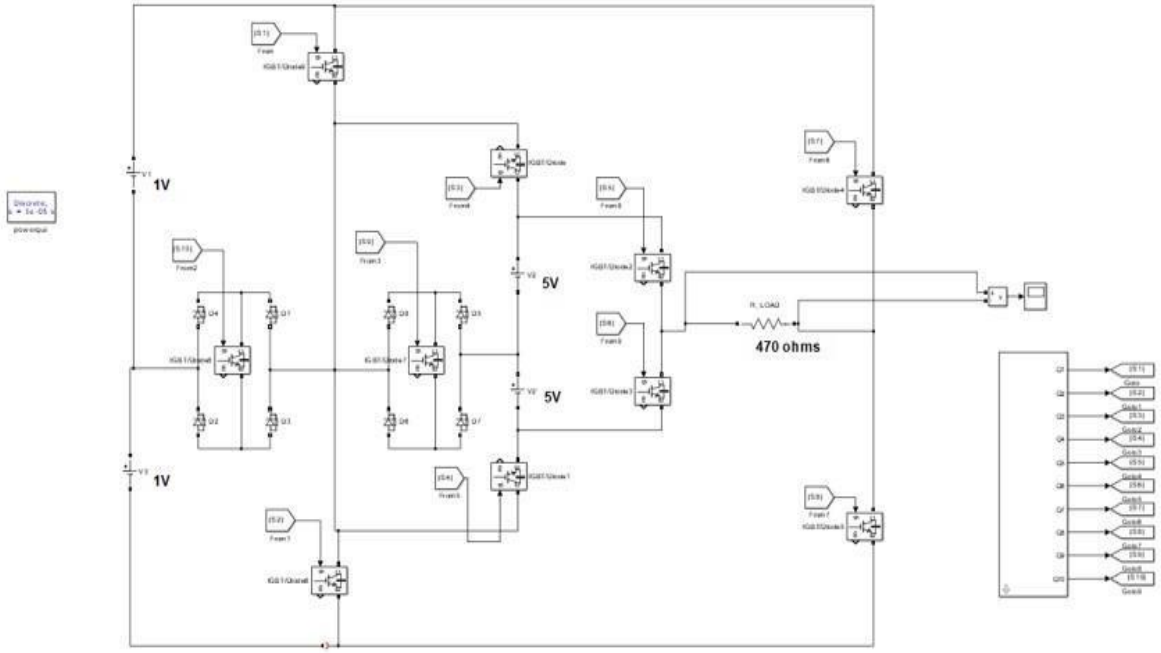


Figure 1.2. Simulation Model of Proposed System

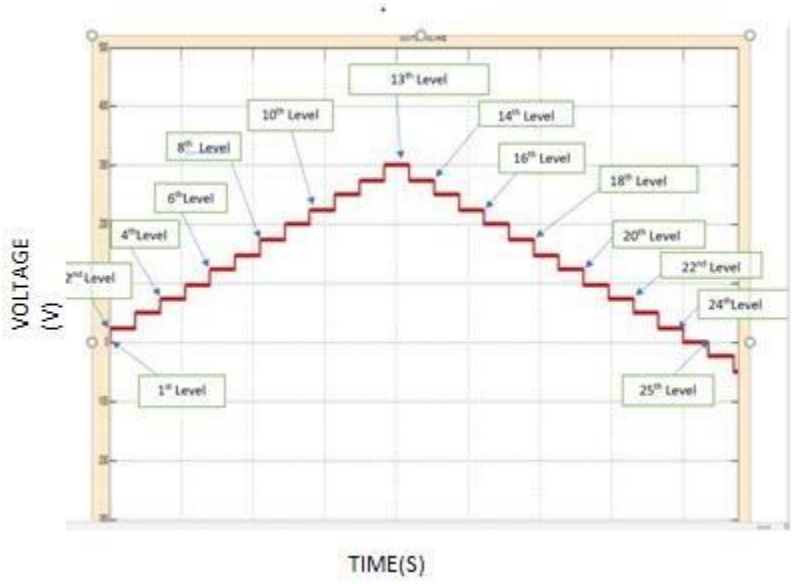
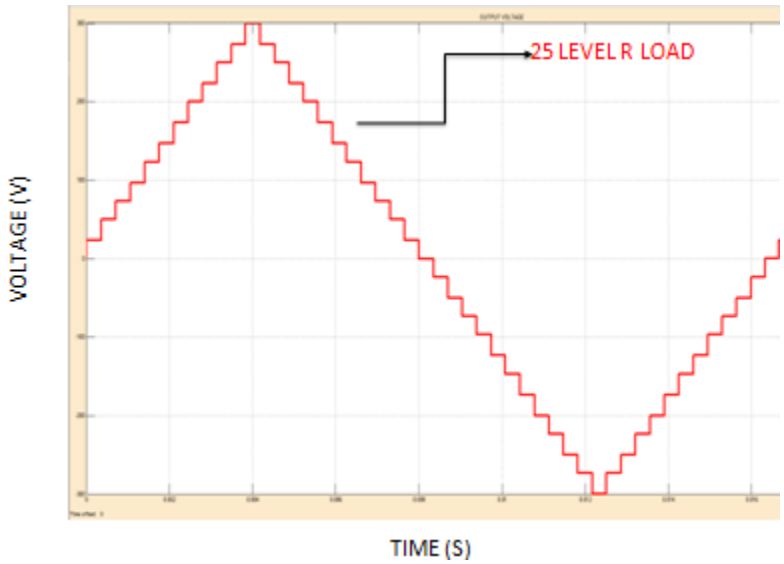


Figure 1.3. Simulation Result For 1 Cycle Of 25 Level Inverter



TDH Analysis

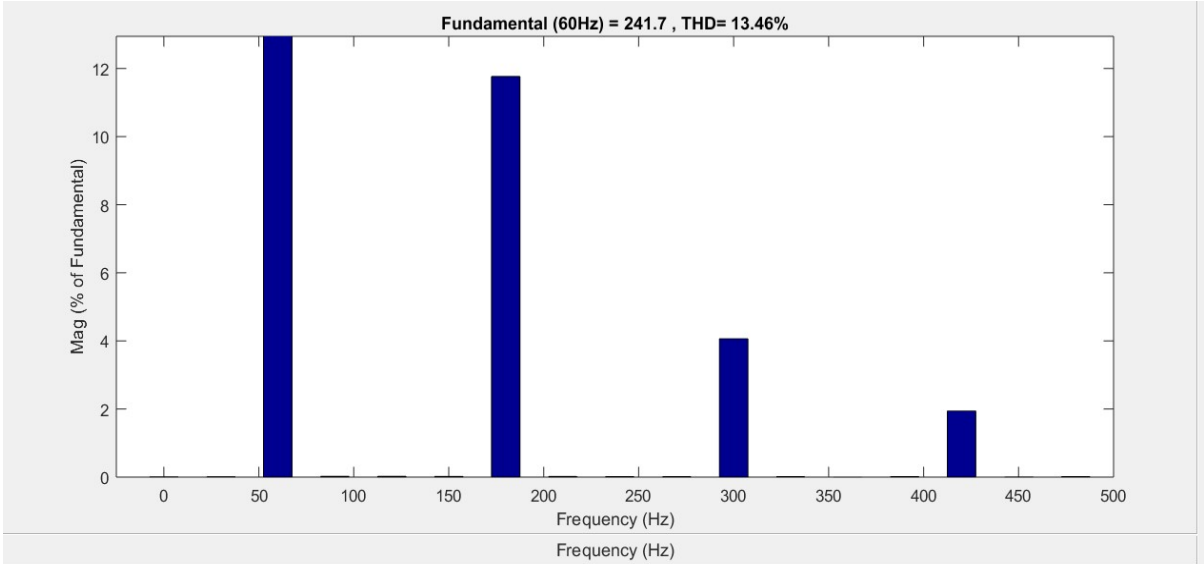


Figure 1.5. THD Analysis of resistive load

The THD analysis of 4S-25 level has been analyzed and the THD value obtained is about 13.46% for a R load of 470Ω.

IMPLEMENTATION

The hardware circuit diagram shown in fig 6 is developed as an experimental prototype and itis depicted in Fig.7. The setup uses four sources and ten switches and it is tested with 470Ω resistive load. The experimentation yields 25-L at the resistive load and it is captured in CRO shown in fig 8. Hence the staircase output voltage of the 25-Level is generated with minimum components count.

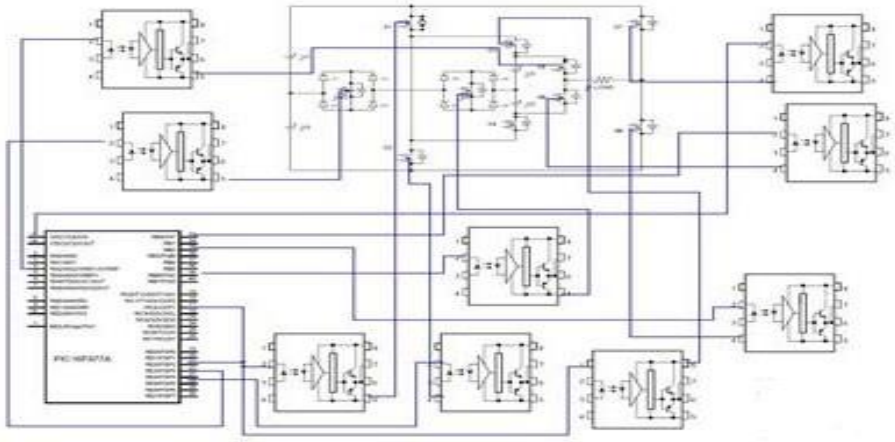


Figure 1.6. Hardware circuit diagram

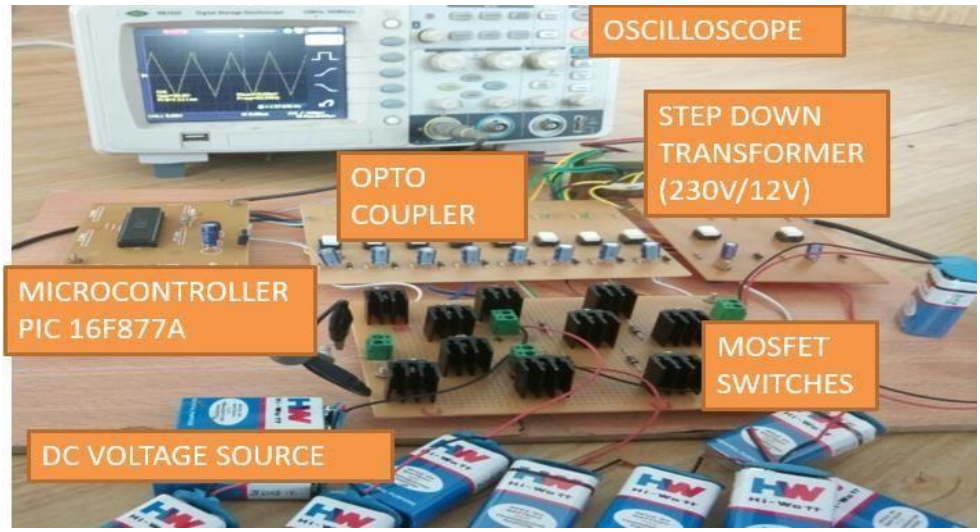


Figure 1.7. The Inverter Topology Experimented with R Load (R=470Ω)

Figure 1.8. Output voltage of 25 level inverter with R Load (R=470Ω)

RESULTS

Based on the tests done, the output is measured and found to be matching with the experimental values. The simulation study also taken and every result are found to be coherent.

CONCLUSION

The presented design yields 25-L at the output. The simulation and experimentation work is carried out to view the operation of the inverter. The comparison between experimental and simulation wave forms further confirms the validity of the proposed multilevel inverter Topology is better. This topology can find suitable place in renewable energy applications, toprovide a small sinusoidal waveform at load.

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